In the Claims

Claims 1-2 are canceled.

3. [Previously Presented] A method of forming a conductive capacitor plug in a memory array, the method comprising extending conductive material from proximate a substrate node location to a location elevationally above all conductive material of an adjacent bit line, wherein the extending comprises etching a contact opening through insulative material after forming said bit line and forming conductive material within the contact opening, wherein the forming of the conductive material comprises forming a storage capacitor at least partially within the contact opening.

4. [Previously Presented] The method of claim 3, wherein the extending comprises etching a contact opening through two separately-formed insulative material layers, at least a portion of the contact opening being generally self-aligned to said bit line, and forming conductive material within the contact opening.

5. [Previously Presented] The method of claim 3, wherein the array comprises a word line elevationally below the bit line, and the extending comprises etching a contact opening through insulative material and generally self-aligned to both said bit line and said word line.

6. [Original] The method of claim 5, wherein the insulative material comprises two or more separately-formed insulative material layers.

7. [Previously Presented] The method of claim 3, wherein the extending comprises:

forming a patterned masking layer over the substrate and defining an opening pattern over said substrate node location;

etching insulative material through the opening pattern sufficient to form a contact opening after forming said bit line; and

forming conductive material within the contact opening.

8. [Original] The method of claim 7, wherein said opening pattern is formed over a plurality of substrate node locations over which individual capacitors are to be formed.

9. [Previously Presented] The method of claim 3, wherein said substrate node location comprises a diffusion region, and the extending comprises:

etching a contact opening through insulative material to substantially expose a portion of the diffusion region after forming said bit line; and

forming conductive material within the contact opening and in electrical communication with the diffusion region.

10. [Original] The method of claim 9, wherein said insulative material comprises two separately-formed layers of insulative material.

Claims 11-48 are canceled.

49. [Previously Presented] A method of forming a conductive capacitor plug in a memory array employing shallow trench isolation, the method comprising extending conductive material from proximate a substrate node location to a location elevationally above all conductive material of an adjacent bit line; and

wherein the array comprises a word line elevationally below the bit line, and the extending comprises etching a contact opening through insulative material and generally self-aligned to both said bit line and said word line.

50. [Previously Presented] The method of claim 49, wherein the extending comprises etching a contact opening through insulative material after forming said bit line and forming conductive material within the contact opening.

51. [Previously Presented] The method of claim 50, wherein the forming of the conductive material comprises forming a storage capacitor at least partially within the contact opening.

52. [Previously Presented] The method of claim 49, wherein the extending comprises etching a contact opening through two separately-formed insulative material layers, at least a portion of the contact opening being generally self-aligned to said bit line, and forming conductive material within the contact opening.

53. [Previously Presented] The method of claim 49, wherein the insulative material comprises two or more separately-formed insulative material layers.

54. [Previously Presented] The method of claim 49, wherein the extending comprises:

forming a patterned masking layer over the substrate and defining an opening pattern over said substrate node location;

etching insulative material through the opening pattern sufficient to form a contact opening after forming the bit line; and

forming conductive material within the contact opening.

55. [Previously Presented] The method of claim 54, wherein the opening pattern is formed over a plurality of substrate node locations over which individual capacitors are to be formed.

56. [Previously Presented] The method of claim 49, wherein the substrate node location comprises a diffusion region, and the extending comprises:

etching a contact opening through insulative material to substantially expose a portion of the diffusion region after forming the bit line; and

forming conductive material within the contact opening and in electrical communication with the diffusion region.

57. [Previously Presented] The method of claim 56, wherein the insulative material comprises two separately-formed layers of insulative material.

58. [Previously Presented] The method of claim 3, wherein the forming the storage capacitor at least partially within the contact opening comprises forming electrically conductive and electrically insulative material of the storage capacitor within the contact opening.

Claims 59-60 are canceled.

Cancel claims 61-62.

63. [Previously Presented] The method of claim 3 wherein the forming the conductive material comprises forming a first electrode of the storage capacitor, and further comprising forming a dielectric layer of the storage capacitor within the contact opening and configured to insulate the first electrode from a second electrode of the storage capacitor.

64. [Previously Presented] The method of claim 63 further comprising forming at least a portion of the second electrode within the contact opening.

65. [Previously Presented] The method of claim 49 wherein the extending the conductive material comprises forming a first electrode of the storage capacitor, and further comprising forming a dielectric layer of the storage capacitor within the contact opening and configured to insulate the first electrode from a second electrode of the storage capacitor.

66. [Previously Presented] The method of claim 65 further comprising forming at least a portion of the second electrode within the contact opening.